

ESP32-C3 Family

Hardware Design Guidelines



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Espressif Systems
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About This Document

The guidelines outline recommended design practices when developing standalone or add-on systems based on the ESP32-C3 series of products, including ESP32-C3 SoCs, ESP32-C3 modules and ESP32-C3 development boards.

Document Updates

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Revision History

For the revision history of this document, please refer to the [last page](#).

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1. Overview

ESP32-C3 family is an ultra-low-power MCU-based SoC solution that supports 2.4 GHz Wi-Fi and Bluetooth® Low Energy (Bluetooth LE). With its state-of-the-art power and RF performance, this SoC is an ideal choice for a wide variety of application scenarios relating to Internet of Things (IoT), smart home, industrial automation, health care, and consumer electronics.

At the core of this chip is a 32-bit RISC-V single-core processor that operates at up to 160 MHz. The chip supports application development, without the need for a host MCU.

ESP32-C3 family provides a highly-integrated way to implement Wi-Fi and Bluetooth LE technologies using a complete RF subsystem, including an antenna switch, RF balun, power amplifier, low noise amplifier (LNA), filter, power management unit, calibration circuits, etc. As a result, PCB size has been greatly reduced.

With its advanced calibration circuitry, ESP32-C3 can dynamically adjust itself to remove external circuit imperfections or adapt to changes in external conditions. As such, the mass production of ESP32-C3 family does not require expensive and specialized Wi-Fi test equipment.

For more information about ESP32-C3 family, please refer to [ESP32-C3 Family Datasheet](#).

2. Schematic Checklist

Thanks to high integration, ESP32-C3 family has simpler peripheral circuit design. The core circuit requires about 20 resistors, capacitors and inductors in total, as well as 1 crystal and 1 SPI flash. This document explains in detail the schematics and PCB layout of ESP32-C3 family.

Figure 1 shows the core circuit of ESP32-C3 family.

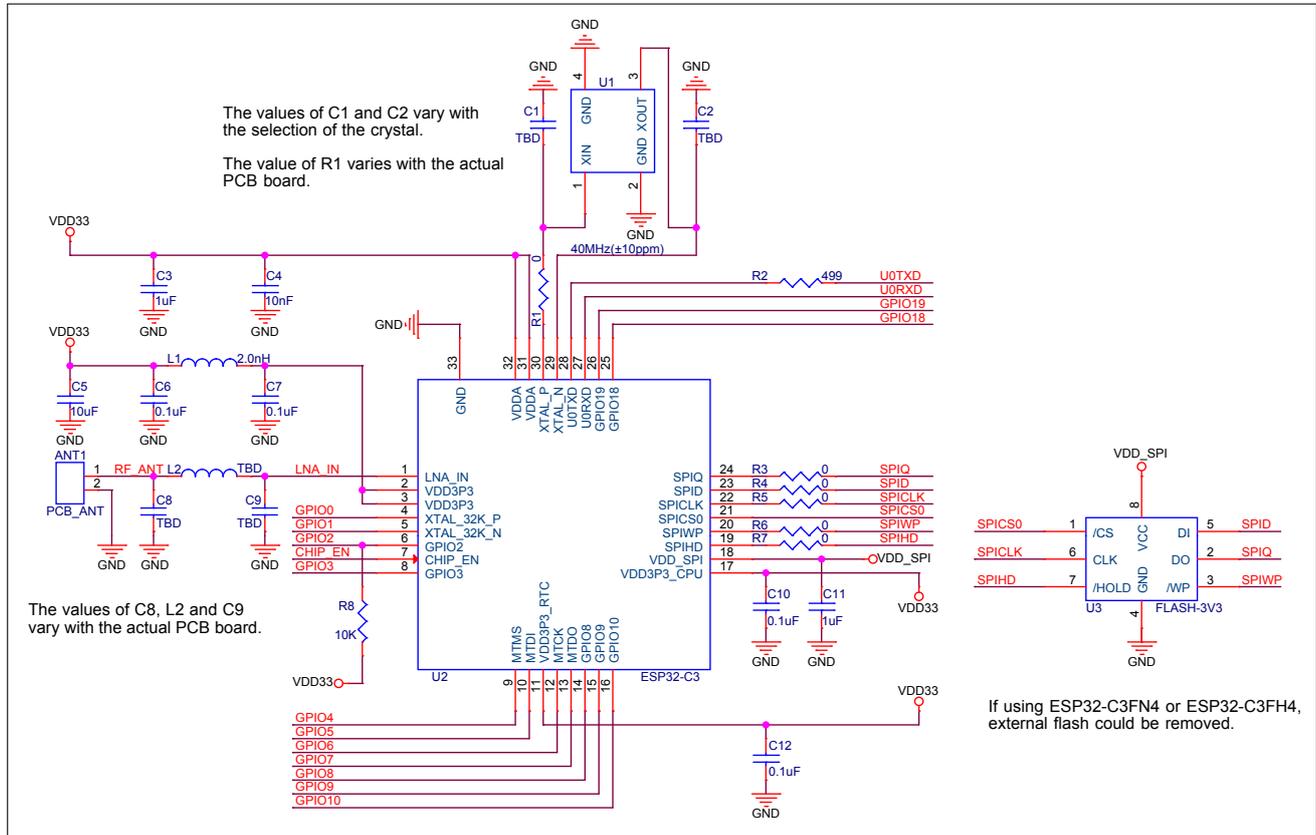


Figure 1: ESP32-C3 Family Schematic

Highlights in ESP32-C3 family circuit design may be broken down into nine major sections:

- Power supply
- Power-on sequence and system reset
- Flash
- Clock source
- RF
- UART
- ADC
- Strapping pins
- GPIO

2.1 Power Supply

For details of using power supply pins, please refer to Section *Power Scheme* in [ESP32-C3 Family Datasheet](#).

2.1.1 Digital Power Supply

Pin 11 and pin 17 are the power supply pins for RTC IO and CPU IO respectively, in a voltage range of 3.0 V ~ 3.6 V. We recommend adding 0.1 μ F capacitors close to each digital power supply pin.

When working as an output power supply pin, VDD_SPI can be powered by VDD3P3_CPU via R_{SPI} (nominal 3.3 V). Therefore, there will be a voltage drop on VDD_SPI to VDD3P3_CPU. We recommend adding a 1 μ F filter capacitor between VDD_SPI and ground.

When not working as a power supply pin, VDD_SPI can be used as GPIO11.

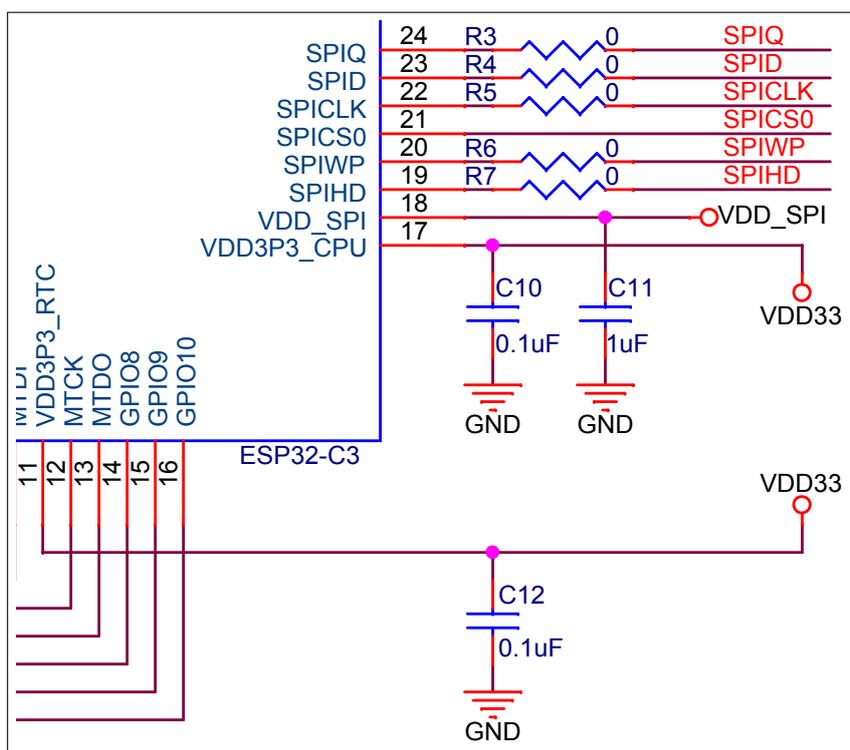


Figure 2: ESP32-C3 Family Digital Power Supply Pins

Notice:

When VDD_SPI works as the power supply pin for embedded and external 3.3 V flash, VDD3P3_CPU should be 3.0 V or above, so as to fall into flash's operating voltage range.

2.1.2 Analog Power Supply

Pin 2, pin 3, pin 31, and pin 32 are the analog power supply pins, working at 3.0 V ~ 3.6 V. Please note that when ESP32-C3 family works in transmission (TX) mode, the instantaneous current is higher and may cause a power rail collapse. Therefore, it is highly recommended to add a 10 μ F capacitor to the power trace, which can work in conjunction with the 0.1 μ F capacitor. In addition, a LC filter circuit needs to be added near pin 2 and pin 3 to suppress high-frequency harmonics. The inductor's rated current is preferably 500 mA or above. Refer to Figure 3 and place the appropriate decoupling capacitor near each analog power pin.

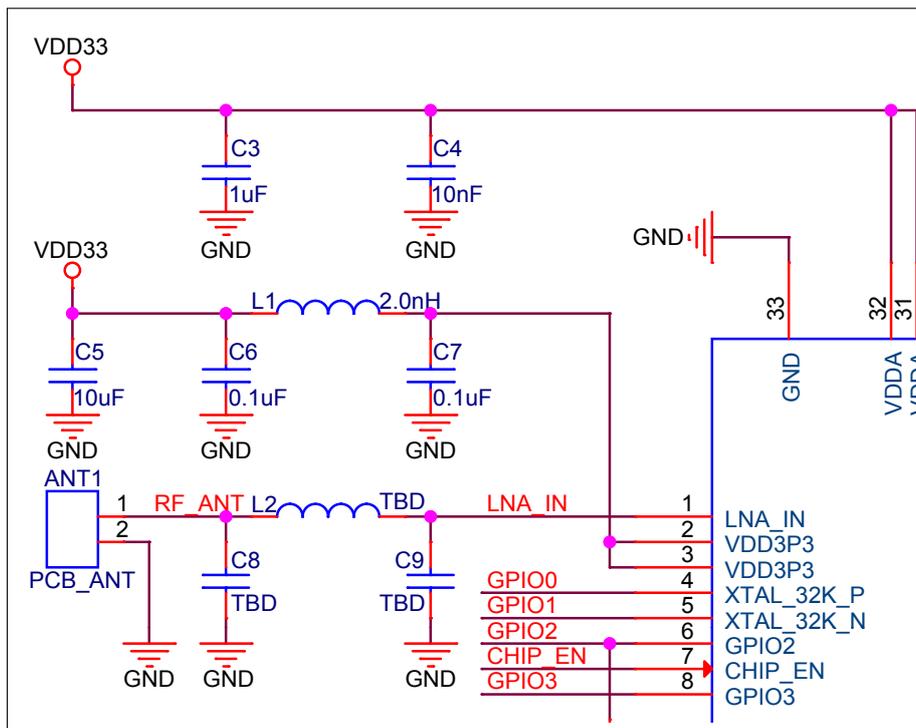


Figure 3: ESP32-C3 Family Analog Power Supply Pins

Notice:

- If you use a single power supply, the recommended voltage of the power supply for ESP32-C3 family is 3.3 V, and its recommended output current is 500 mA or more.
- You are suggested to add an ESD protection diode at the power entrance.

2.2 Power-on Sequence and System Reset

2.2.1 Power-on Sequence

ESP32-C3 family uses a 3.3 V system power supply. The chip should be activated after the power rails have stabilized. This is achieved by delaying the activation of pin 7 CHIP_EN after the 3.3 V rails have been brought up.

Figure 4 shows the power-up and reset timing of ESP32-C3 family. Details about the parameters are listed in Table 1.

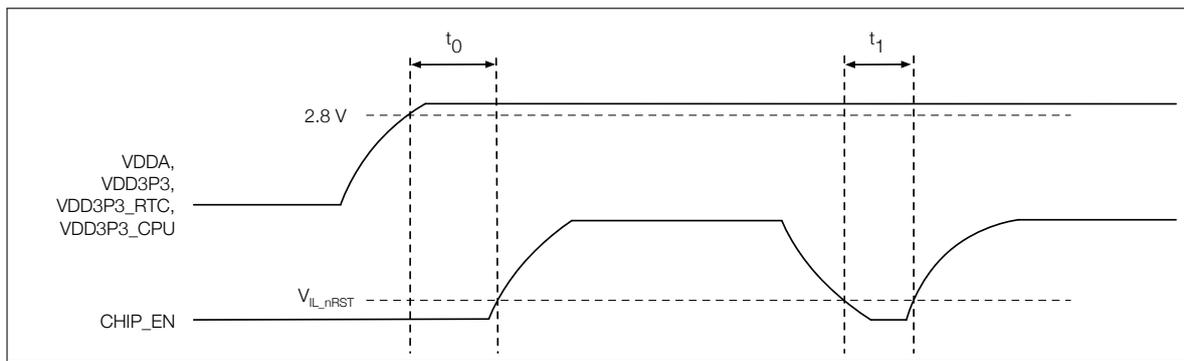


Figure 4: ESP32-C3 Family Power-up and Reset Timing

Table 1: Description of ESP32-C3 Family Power-up and Reset Timing Parameters

Parameter	Description	Min (μs)
t_0	Time between bringing up the VDDA, VDD3P3, VDD3P3_RTC, and VDD3P3_CPU rails, and activating CHIP_EN	50
t_1	Duration of CHIP_EN signal level $< V_{IL_nRST}$ to reset the chip	50

Notice:

To ensure the power supply to the ESP32-C3 family chip is stable during power-up, it is advised to add an RC delay circuit at the CHIP_EN pin. The recommended setting for the RC delay circuit is usually $R = 10\text{ k}\Omega$ and $C = 1\ \mu\text{F}$. However, specific parameters should be adjusted based on the power-up timing of the power supply and the power-up and reset sequence timing of the chip.

2.2.2 Reset

CHIP_EN can be used as the reset pin of ESP32-C3 family. When CHIP_EN is at low level, the reset voltage (V_{IL_nRST}) should be $(-0.3 \sim 0.25 \times VDD)\text{ V}$ (where VDD is the I/O voltage for a particular power domain of pins). To avoid reboots caused by external interference, route the CHIP_EN trace as short as possible, and add a pull-up resistor as well as a capacitor to ground whenever possible.

Notice:

CHIP_EN pin must not be left floating.

2.3 Flash

ESP32-C3 family can support up to 16 MB external flash. The ESP32-C3-WROOM-02 module uses a 4 MB SPI flash, powered by VDD_SPI. We recommend reserving a serial resistor (initially of $0\ \Omega$) on the SPI line, to lower the driving current, adjust timing, reduce crosstalk and external interference, etc.

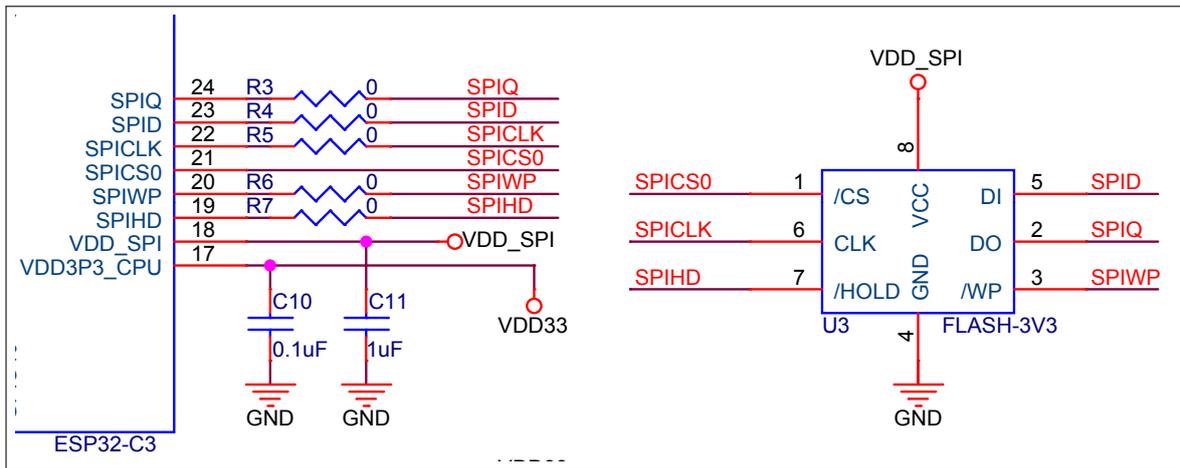


Figure 5: ESP32-C3 Family Flash Circuit

2.4 Clock Source

There are two clock sources for ESP32-C3 family, namely an external crystal clock source and an RTC clock source.

2.4.1 External Clock Source (compulsory)

Currently, the ESP32-C3 family firmware only supports 40 MHz crystal. The specific capacitance of C1 and C2 depends on further testing of, and adjustment to, the overall performance of the whole circuit. Please add a component in series on the XTAL_P clock trace to reduce the drive capability of the crystal and to minimize the impact of crystal harmonics on RF performance. The value of this component (initially of 24 nH) depends on further testing. Note that the accuracy of the selected crystal needs to be ± 10 ppm.

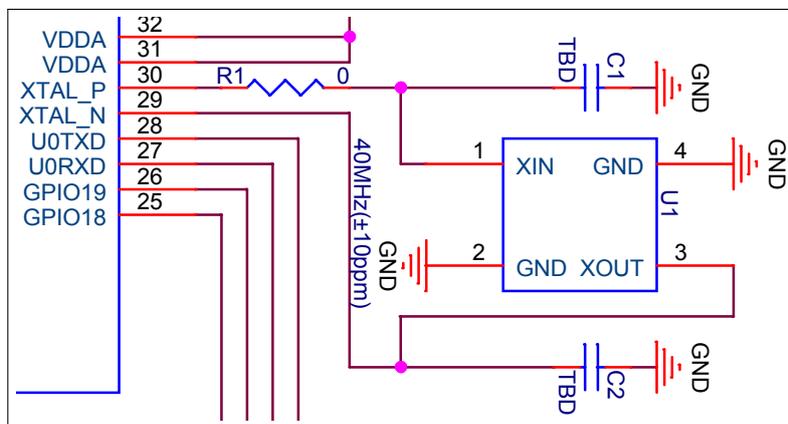


Figure 6: Schematic for ESP32-C3 Family's Crystal

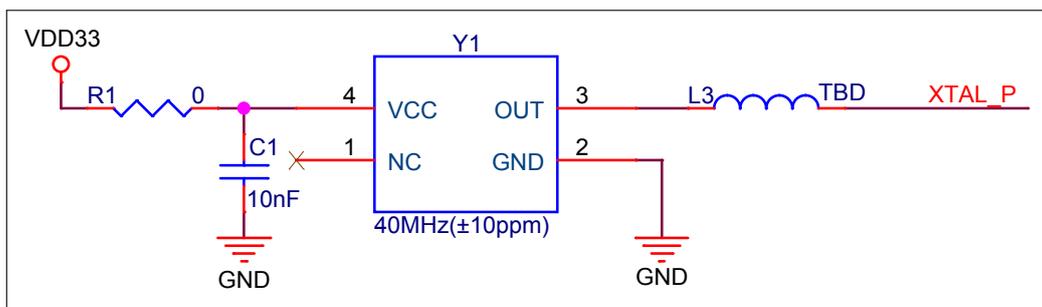


Figure 7: Schematic for ESP32-C3 Family's Oscillator

Notice:

- If you use an oscillator, its output should be connected to XTAL_P on the chip through a series inductor (initially of 20 nH). XTAL_N can be floating. Please make sure that the oscillator output is stable and its accuracy is within ± 10 ppm. It is also recommended that the circuit design for the oscillator is compatible with the use of crystal, in case that if there is a problem with oscillator circuit, the oscillator can be replaced by the crystal.
- Although ESP32-C3 family has calibration circuits, defects in the crystal itself (for example, large frequency deviation of more than ± 10 ppm, unstable performance over operating temperature range, etc) may lead to the malfunction of ESP32-C3 family, resulting in RF performance degradation.

2.4.2 RTC Clock (optional)

ESP32-C3 family supports an external 32.768 kHz crystal to act as the RTC sleep clock.

Figure 8 shows the schematic for the external 32.768 kHz crystal.

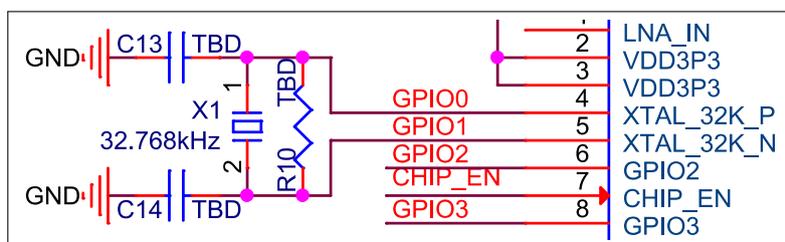


Figure 8: Schematic for ESP32-C3 Family's External Crystal (RTC)

Notice:

- Requirements for the 32.768 kHz crystal:
 - Equivalent series resistance (ESR) ≤ 70 k Ω .
 - Load capacitance at both ends should be configured according to the crystal's specification.
- The parallel resistor R10 is used for biasing the crystal circuit (5 M Ω $<$ R12 ≤ 10 M Ω). In general, you do not need to populate R10.
- If the RTC source is not required, then pin 4 (XTAL_32K_P) and pin 5 (XTAL_32K_N) can be used as general GPIOs.

2.5 RF

In your circuit design, please add a π -matching network for antenna matching, preferably a CLC network.

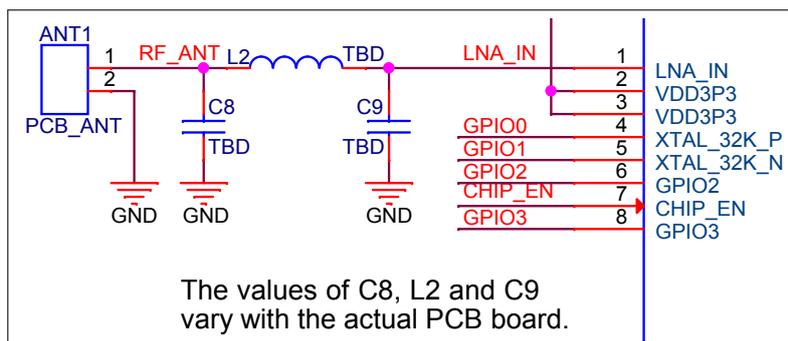


Figure 9: ESP32-C3 Family RF Matching Schematic

Note:

The parameters of the components in the matching network are subject to the actual antenna and PCB layout.

2.6 UART

You need to connect a 499 Ω resistor to the U0TXD line to suppress the 80 MHz harmonics.

2.7 ADC

It is recommended to add a 0.1 μF filter capacitor between pins and ground when using the ADC function. Please note that ADC2 is not factory-calibrated. We recommend using ADC1.

2.8 Strapping Pins

Note:

The content below is excerpted from Section Strapping Pins in [ESP32-C3 Family Datasheet](#).

ESP32-C3 family has three strapping pins:

- GPIO2
- GPIO8
- GPIO9

Software can read the values of GPIO2, GPIO8 and GPIO9 from GPIO_STRAPPING field in GPIO_STRAP_REG register. For register description, please refer to Section GPIO Matrix Register Summary in [ESP32-C3 Technical Reference Manual](#).

During the chip's system reset, the latches of the strapping pins sample the voltage level as strapping bits of "0" or "1", and hold these bits until the chip is powered down or shut down.

Types of system reset include:

- power-on-reset
- RTC watchdog reset
- brownout reset
- analog super watchdog reset
- crystal clock glitch detection reset

By default, GPIO9 is connected to the internal pull-up resistor. If GPIO9 is not connected or connected to an external high-impedance circuit, the latched bit value will be "1"

To change the strapping bit values, you can apply the external pull-down/pull-up resistances, or use the host MCU's GPIOs to control the voltage level of these pins when powering on ESP32-C3 family.

After reset, the strapping pins work as normal-function pins.

Refer to Table 2 for a detailed boot-mode configuration of the strapping pins.

Table 2: Strapping Pins

Booting Mode ¹			
Pin	Default	SPI Boot	Download Boot
GPIO2	N/A	1	1
GPIO8	N/A	Don't care	1
GPIO9	Internal pull-up	1	0
Enabling/Disabling ROM Code Print During Booting			
Pin	Default	Functionality	
GPIO8	N/A	When the value of eFuse field EFUSE_UART_PRINT_CONTROL is 0 (default), print is enabled and not controlled by GPIO8. 1, if GPIO8 is 0, print is enabled; if GPIO8 is 1, it is disabled. 2, if GPIO8 is 0, print is disabled; if GPIO8 is 1, it is enabled. 3, print is disabled and not controlled by GPIO8.	

¹ The strapping combination of GPIO8 = 0 and GPIO9 = 0 is invalid and will trigger unexpected behavior.

Figure 10 shows the setup and hold times for the strapping pin before and after the CHIP_EN signal goes high. Details about the parameters are listed in Table 3.

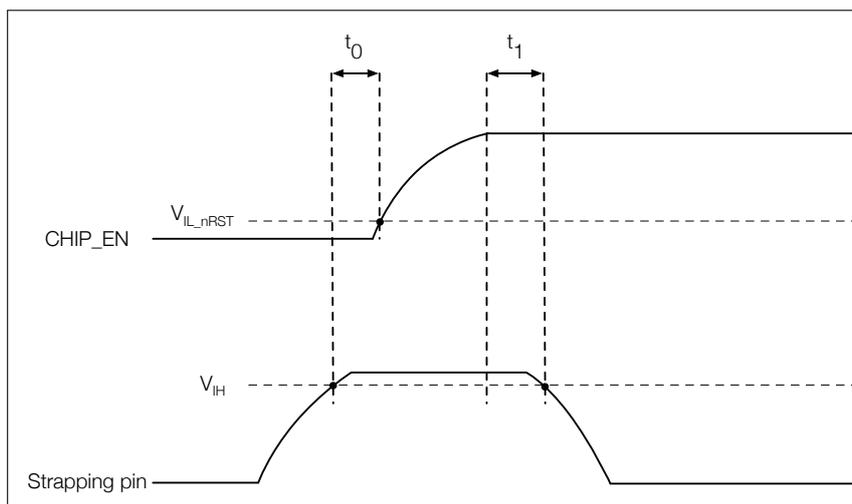


Figure 10: Setup and Hold Times for the Strapping Pin

Table 3: Parameter Descriptions of Setup and Hold Times for the Strapping Pin

Parameter	Description	Min (ms)
t_0	Setup time before CHIP_EN goes from low to high	0
t_1	Hold time after CHIP_EN goes high	3

2.9 GPIO

Note:

The content below is excerpted from Section General Purpose Input / Output Interface (GPIO) in [ESP32-C3 Family Datasheet](#).

ESP32-C3 family has 22 GPIO pins which can be assigned various functions by configuring corresponding registers. Besides digital signals, some GPIOs can be also used for analog functions, such as ADC.

All GPIOs have selectable internal pull-up or pull-down, or can be set to high impedance. When these GPIOs are configured as an input, the input value can be read by software through the register. Input GPIOs can also be set to generate edge-triggered or level-triggered CPU interrupts. All digital IO pins are bi-directional, non-inverting and tristate, including input and output buffers with tristate control. These pins can be multiplexed with other functions, such as the UART, SPI, etc. For low-power operations, the GPIOs can be set to holding state.

The IO MUX and the GPIO matrix are used to route signals from peripherals to GPIO pins. Together they provide highly configurable I/O. Using GPIO Matrix, peripheral input signals can be configured from any IO pins while peripheral output signals can be configured to any IO pins. Table 4 shows the IO MUX functions of each pin. For more information about IO MUX and GPIO matrix, please refer to Chapter IO MUX and GPIO Matrix (GPIO, IO_MUX) in [ESP32-C3 Technical Reference Manual](#).

Table 4: IO MUX Pin Functions

Name	No.	Function 0	Function 1	Function 2	Reset	Notes
XTAL_32K_P	4	GPIO0	GPIO0	—	0	R

Name	No.	Function 0	Function 1	Function 2	Reset	Notes
XTAL_32K_N	5	GPIO1	GPIO1	—	0	R
GPIO2	6	GPIO2	GPIO2	FSPIQ	1	R
GPIO3	8	GPIO3	GPIO3	—	1	R
MTMS	9	MTMS	GPIO4	FSPIHD	1	R
MTDI	10	MTDI	GPIO5	FSPIWP	1	R
MTCK	12	MTCK	GPIO6	FSPICLK	1*	G
MTDO	13	MTDO	GPIO7	FSPID	1	G
GPIO8	14	GPIO8	GPIO8	—	1	—
GPIO9	15	GPIO9	GPIO9	—	3	—
GPIO10	16	GPIO10	GPIO10	FSPICS0	1	G
VDD_SPI	18	GPIO11	GPIO11	—	0	—
SPIHD	19	SPIHD	GPIO12	—	3	—
SPIWP	20	SPIWP	GPIO13	—	3	—
SPICS0	21	SPICS0	GPIO14	—	3	—
SPICLK	22	SPICLK	GPIO15	—	3	—
SPID	23	SPID	GPIO16	—	3	—
SPIQ	24	SPIQ	GPIO17	—	3	—
GPIO18	25	GPIO18	GPIO18	—	0	USB, G
GPIO19	26	GPIO19	GPIO19	—	0*	USB
U0RXD	27	U0RXD	GPIO20	—	3	G
U0TXD	28	U0TXD	GPIO21	—	4	—

Reset

The default configuration of each pin after reset:

- **0** - input disabled, in high impedance state (IE = 0)
- **1** - input enabled, in high impedance state (IE = 1)
- **2** - input enabled, pull-down resistor enabled (IE = 1, WPD = 1)
- **3** - input enabled, pull-up resistor enabled (IE = 1, WPU = 1)
- **4** - output enabled, pull-up resistor enabled (OE = 1, WPU = 1)
- **0*** - input disabled, pull-up resistor enabled (IE = 0, WPU = 0, USB_WPU = 1). See details in Notes
- **1*** - When the value of eFuse bit EFUSE_DIS_PAD_JTAG is
 - 0, input enabled, pull-up resistor enabled (IE = 1, WPU = 1)
 - 1, input enabled, in high impedance state (IE = 1)

We recommend pulling high or low GPIO pins in high impedance state to avoid unnecessary power consumption. You may add pull-up and pull-down resistors in your PCB design referring to Table DC Characteristics (3.3 V, 25 °C) in [ESP32-C3 Family Datasheet](#), or enable internal pull-up and pull-down resistors during software initialization.

Notes

- **R** - These pins have analog functions.

- **USB** - GPIO18 and GPIO19 are USB pins. The pull-up value of a USB pin is controlled by the pin's pull-up value together with USB pull-up value. If any of the two pull-up values is 1, the pin's pull-up resistor will be enabled. The pull-up resistors of USB pins are controlled by USB_SERIAL_JTAG_DP_PULLUP bit.
- **G** - These pins have glitches during power-up. See details in Table 5.

Table 5: Power-Up Glitches on Pins

Pin	Glitch ¹	Typical Time Period (ns)
MTCK	Low-level glitch	5
MTDO	Low-level glitch	5
GPIO10	Low-level glitch	5
U0RXD	Low-level glitch	5
GPIO18	Pull-up glitch	50000

¹ Low-level glitch: the pin is at a low level during the time period;
High-level glitch: the pin is at a high level during the time period;
Pull-up glitch: the pin is pulled up during the time period;
Pull-down glitch: the pin is pulled down during the time period.

3. PCB Layout Design

This chapter takes ESP32-C3-WROOM-02 module as an example to illustrate key points of ESP32-C3 family PCB layout.

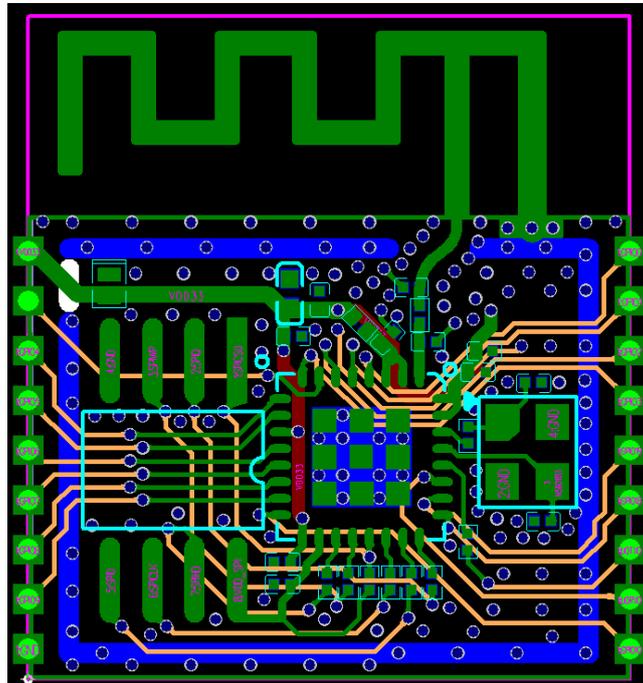


Figure 11: ESP32-C3 Family PCB Layout

3.1 General Principles of PCB Layout

We recommend a four-layer PCB design.

- The first layer is the TOP layer for signal traces and components.
- The second layer is the GND layer without signal traces being routed so as to ensure a complete GND plane.
- The third layer is the POWER layer where a GND plane should be applied to better isolate the RF module and crystal. It is acceptable to route signal traces on this layer, provided that there is a complete GND plane under the RF module and crystal.
- The fourth layer is the BOTTOM layer, where power traces are routed. It is not recommended to place any components on this layer.

Below are the suggestions for a two-layer PCB design.

- The first layer is the TOP layer for traces and components.
- The second layer is the BOTTOM layer. Please do not place any components on this layer and keep traces to a minimum. Ideally, it should be a complete GND plane.

3.2 Placement of Module on the Base Board

If you design an on-board module, please pay attention to the placement of the module on the base board. The aim is to minimize the impact of the base board on the module's antenna performance.

The module should be placed as close to the edge of the base board as possible. The PCB antenna area should be placed outside the base board whenever possible. In addition, the feed point of the antenna should be closest to the board, as shown in Figure 13 and Figure 12.

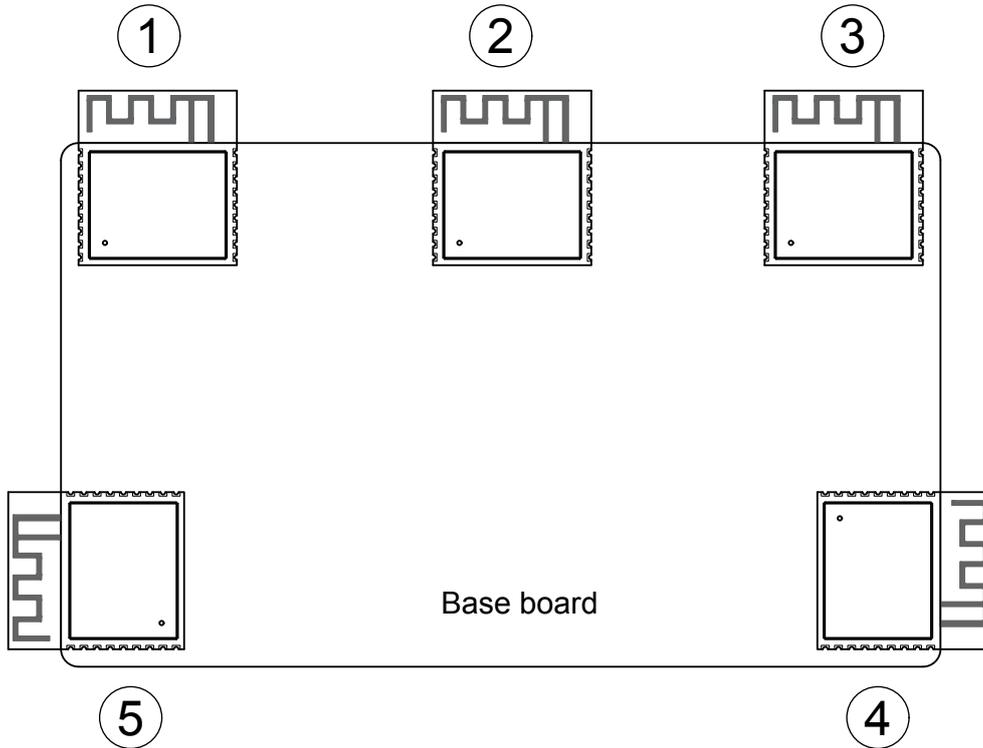


Figure 12: Placement of ESP32-C3 Modules on Base Board. Antenna Feed Point on the Right

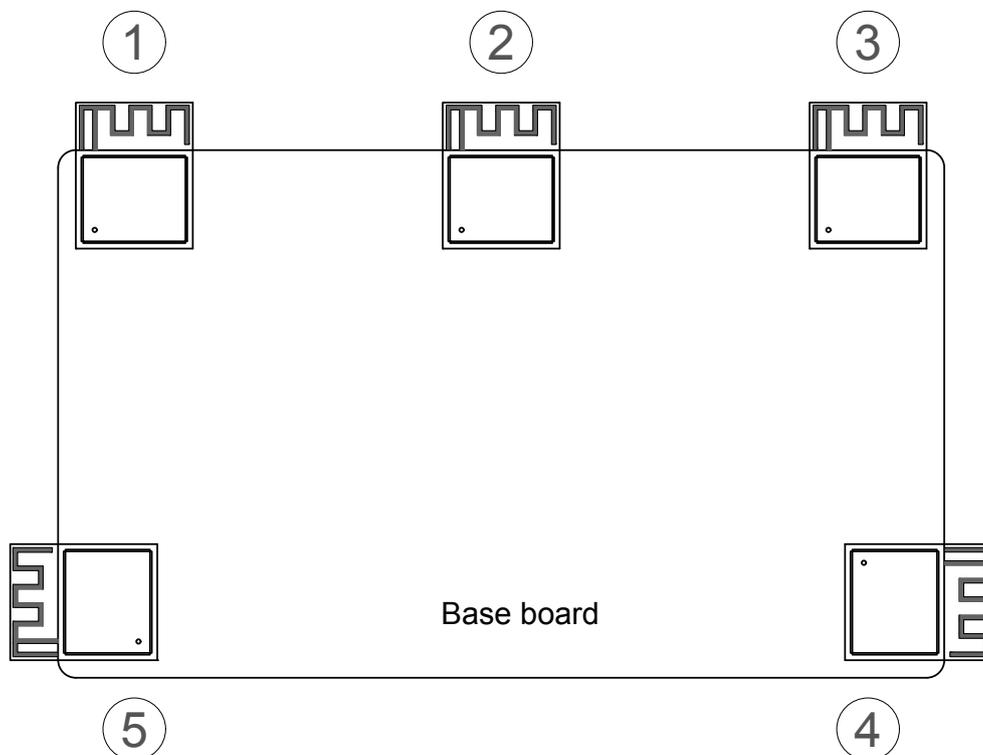


Figure 13: Placement of ESP32-C3 Modules on Base Board. Antenna Feed Point on the Left

Note:

In Figure 12, the recommended position of ESP32-C3 modules (feed point on the right) on the base board should be:

- Position 3, 4: Highly recommended;
- Position 1, 2, 5: Not recommended.

In Figure 13, the recommended position of ESP32-C3 modules (feed point on the left) on the base board should be:

- Position 1, 5: Highly recommended;
- Position 2, 3, 4: Not recommended.

If the positions recommended are not feasible, please make sure that the module is not covered by any metal shell. Besides, the antenna area of the module and the area 15 mm outside the antenna should be kept clean, (namely no copper, routing, components on it) as shown in Figure 14.

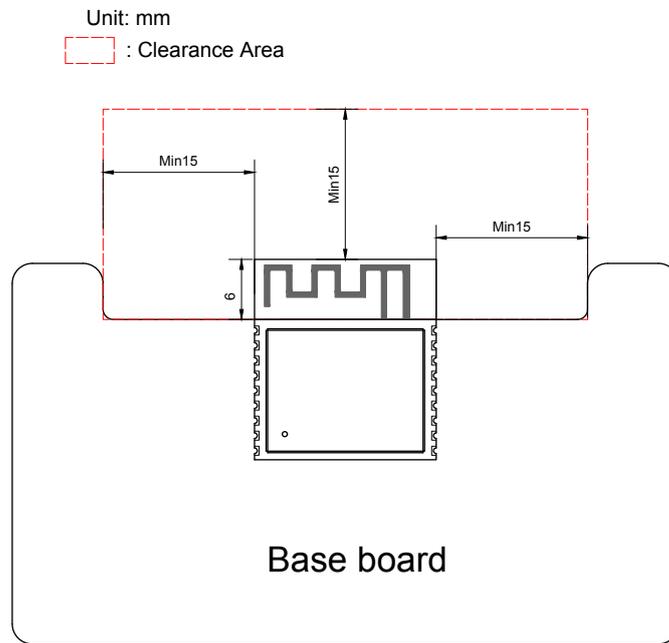


Figure 14: Keepout Zone for ESP32-C3 Module's Antenna on the Base Board

If there is base board under the antenna area, it is recommended to cut it off to minimize its impact on the antenna. When designing an end product, pay attention to the impact of enclosure on the antenna.

3.3 Power Supply

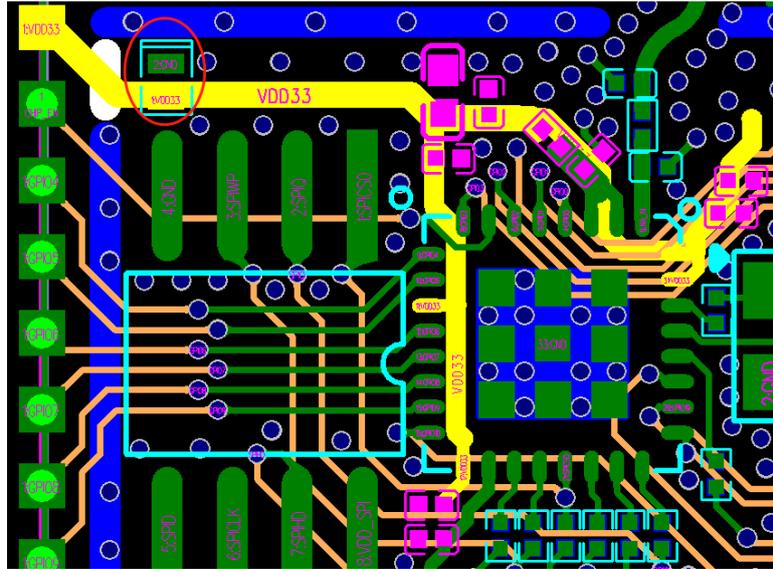


Figure 15: ESP32-C3 Family Power Traces in a Four-layer PCB Design

- Four-layer PCB design is recommended over two-layer design. Route the power traces on the fourth (bottom) layer whenever possible. Vias are required for the power traces to go through the layers and get connected to the pins on the top layer. There should be at least two vias if the main power traces need to cross layers. The drill diameter on other power traces should be no smaller than the width of the power traces.
- As shown in Figure 15, an ESD protection diode is placed close to the power port (marked in red circle). A 10 μF capacitor is required before the power trace is connected to the chip, to be used in conjunction with a 0.1 μF capacitor. Then the power traces are divided into two ways from here and form a star-shape topology, thus reducing the coupling between different power pins. Note that all decoupling capacitors should be placed close to the power pin, and ground vias should be added close to the ground pin of decoupling capacitors to ensure a short return path.
- The 3.3 V power traces, highlighted in yellow, are routed as shown in Figure 15. The width of the main power traces should be at least 20 mil. The width of the power traces for pin 2 and pin 3 should be at least 15 mil. The width of other power traces is preferably 10 mil.
- As shown in Figure 16, we recommend connecting the capacitor to ground in the LC filter circuit near pin 2 and pin 3 (analog power supply pins) to the third and fourth layer through a via, and maintaining a keep-out area on other layers.

- The RF trace should be routed on the outer layer without vias, i.e., should not cross layers. The RF trace should be routed at a 135° angle, or with circular arcs if trace bends are required.
- Please place the π -matching network in a zigzag. For 0201 package, please add a stub between the ground and the two capacitors in parallel to curb second harmonics. It is preferable to keep the stub length 15 mil, and determine the stub width according to the number of PCB layers, so that the characteristic impedance of the stub is $100 \Omega \pm 10\%$. In addition, please connect the stub via to the third layer, and maintain a keep-out area on the first and second layers. If space on PCB is limited, you may add the stub only to parallel capacitors near the chip. The trace highlighted in Figure 16 is the stub.

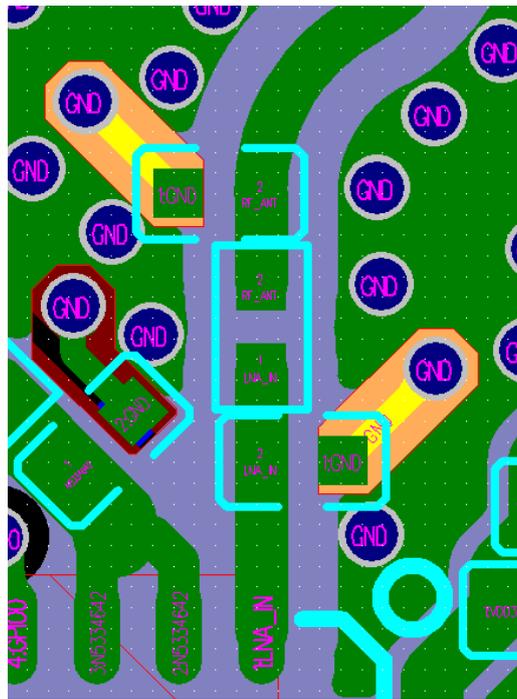


Figure 19: ESP32-C3 RF Stub in a Four-layer PCB Design

- The ground plane on the adjacent layer needs to be complete. Do not route any traces under the RF trace whenever possible.
- There should be no high-frequency signal traces routed close to the RF trace. The RF antenna should be placed away from high-frequency components, such as crystals, DDR, high-frequency clocks, etc. In addition, the USB port, USB-to-serial chip, UART signal lines (including traces, vias, test points, header pins, etc.) must be as far away from the antenna as possible. The UART signal line should be surrounded by ground copper and ground vias .
- For designing the RF trace at 50Ω single-ended impedance, please refer to the PCB stack-up design shown in Figure 20.

3.8 Typical Layout Problems and Solutions

3.8.1 Ripple in the power supply is not large, but the RF transmit (TX) performance is rather poor.

Analysis:

Ripple in the power supply can significantly affect the RF TX performance. Please note that ripple in the power supply must be measured when ESP32-C3 family works in TX mode. Ripple in the power supply changes along with power. The higher the power, the larger the ripple.

Generally, the peak value of the ripple should be < 80 mV when ESP32-C3 family transmits MCS7@11n packets, and < 120 mV when ESP32-C3 family transmits 11m@11b packets.

Solution:

Add a $10 \mu\text{F}$ filter capacitor to the branch of the power trace (the branch routed from the analog power supply pin of ESP32-C3 family). The $10 \mu\text{F}$ capacitor should be as close to the analog power supply pin as possible. The closer the capacitor, the smaller the ripple.

3.8.2 Ripple in power supply is small during packet transmission, but RF TX performance is still poor.

Analysis:

Besides ripple in the power supply, RF TX performance can also be affected by the crystal itself. The following factors will result in poor RF performance:

- Large frequency deviation and other quality issues of the crystal
- Interference from high-frequency signals, e.g. signal coupling resulted from a cross-layer design
- High-frequency signal traces under the crystal, such as UART trace
- Inductive or radiation components around the crystal, such as inductors and antennas

Solution:

This problem is caused by improper PCB layout and can be solved by optimizing the layout. For layout principles, please see Section 3.

3.8.3 When ESP32-C3 family transmits data packets, the measured power is much higher or lower than the target power, and the EVM is relatively poor.

Analysis:

The difference between the measured power and the target power may be due to signal reflection caused by the impedance mismatch on the transmission line connecting the RF pin and the antenna. Besides, the impedance mismatch will affect the working state of the internal PA, making the PA prematurely access the saturated region in an abnormal way. The EVM becomes poor as the signal distortion happens.

Solution:

Match the antenna's impedance with the reserved π circuit on the RF trace, so that impedance of the antenna as seen from the RF pin matches closely with that of the chip. This will reduce reflection to the minimum.

3.8.4 TX performance is not bad, but the RX sensitivity is low.

Analysis:

As TX and RX share the antenna path, good TX performance indicates proper RF impedance matching. The reason of low RX sensitivity might lie in coupling of high-frequency interference signals to the antenna. In this

case, you should consider signal integrity when designing PCB layout.

Solution:

Keep the antenna away from crystals. Do not route high-frequency signal traces close to the RF trace. For details, please see [Section 3](#).

4. Hardware Development

4.1 Modules Built around ESP32-C3 Family of Chips

For a list of ESP32-C3 modules, please check [Modules](#) section of Espressif website.

To review module reference designs, please check [Documentation](#) section of Espressif website.

Notes on Using a Module

- A SMT module uses one single pin as the power supply pin. You only need to connect the module to a 3.3 V power supply that outputs a current of at least 500 mA. The 3.3 V power supply works both for the analog circuit and the digital circuit.
- The EN pin is used for enabling the module. Set the EN pin high when the module is at work. There is no RC delay circuit on the module. It is recommended that users add an external RC delay circuit to the module. For details please refer to Section [2.2](#).
- Lead the GND, RXD, TXD pins out and connect them to a USB-to-UART converter to download firmware, print log, and communicate.

By default, firmware has already been downloaded into the module's flash. If you need to download your own firmware, please follow the steps below:

1. Set the module to UART Download mode by pulling IO9 (pulled up by default) low and IO2 high.
2. Power on the module and check whether the module has entered UART Download mode via serial port.
3. Download your firmware into flash using [Flash Download Tool](#).
4. After firmware has been downloaded, pull IO2 and IO9 high to enter SPI Boot mode.
5. Power on the module again. The chip will read and execute the new firmware during initialization.

Notice:

- During the whole process, you can check the status of the chip by printing log through serial port. If the firmware cannot be downloaded or executed, you can check if the working mode has been configured correctly during the chip initialization by printing log through serial port.
- The serial port cannot be used to print log and download firmware simultaneously.

4.2 Development Boards Built around ESP32-C3 Family of Chips

For latest information about ESP32-C3 development boards, please check [Development Boards](#) section of Espressif website.

Revision History

Date	Version	Release notes
2021-05-28	V1.0	Official release
2021-04-09	V0.5	Preliminary release

Solutions, Documentation and Legal Information

Must-Read Documents

- [ESP32-C3 Family Datasheet](#)
- [ESP32-C3 Technical Reference Manual](#)
- [ESP-IDF Programming Guide](#)
- [Espressif Product Ordering Information](#)
- [Certificates](#)
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